AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-25 (Canceled)

26. (New) A method to facilitate simulating a digital circuit, comprising:

receiving a description of the digital circuit, wherein a first portion of the description is in a hardware description language and a second portion of the description is in a computer programming language,

blending the first portion and the second portion into an executable simulation; and

executing the executable simulation, wherein executing the executable simulation allows a designer to simulate operation of the digital circuit.

27. (New) The method of claim 26, wherein blending the first portion and the second portion involves mapping data types native to the hardware description language to data types native to the computer programming language.

28. (New) The method of claim 26, wherein blending the first portion and the second portion involves creating a wrapper for code written in the computer programming language so that code written in the hardware description language can call code written in the computer programming language.

29. (New) The method of claim 28, wherein the wrapper provides communication mechanisms between code written in the hardware description language and code written in the computer programming language.

30. (New) The method of claim 28, wherein the wrapper is automatically generated.

31. (New) The method of claim 28, wherein the wrapper provides automatic threading.

32. (New) The method of claim 31, wherein automatic threading enables code written in the computer programming language to call code written in the hardware description language.

33. (New) The method of claim 28, wherein the wrapper can output a message upon an occurrence of a call and a return, wherein the message can include values associated with the call and the return.

34. (New) A computer-readable storage medium storing instructions that when executed by a computer cause the computer to perform a method to facilitate simulating a digital circuit, the method comprising:

receiving a description of the digital circuit, wherein a first portion of the description is in a hardware description language and a second portion of the description is in a computer programming language,

blending the first portion and the second portion into an executable simulation; and

executing the executable simulation, wherein executing the executable simulation allows a designer to simulate operation of the digital circuit.

35. (New) The computer-readable storage medium of claim 34, wherein blending the first portion and the second portion involves mapping data types native to the hardware description language to data types native to the computer programming language.

36. (New) The computer-readable storage medium of claim 34, wherein blending the first portion and the second portion involves creating a wrapper for code written in the computer programming language so that code written in the hardware description language can call code written in the computer programming language.

37. (New) The computer-readable storage medium of claim 36, wherein the wrapper provides communication mechanisms between code written in the hardware description language and code written in the computer programming language.

39. (New) The computer-readable storage medium of claim 36, wherein the wrapper is automatically generated.

40. (New) The computer-readable storage medium of claim 36, wherein the wrapper provides automatic threading.

41. (New) The computer-readable storage medium of claim 40, wherein automatic threading enables code written in the computer programming language to call code written in the hardware description language.

42. (New) The computer-readable storage medium of claim 36, wherein the wrapper can output a message upon an occurrence of a call and a return, wherein the message can include values associated with the call and the return.

43. (New) An apparatus to facilitate simulating a digital circuit, comprising:

a receiving mechanism configured to receive a description of the digital circuit, wherein a first portion of the description is in a hardware description language and a second portion of the description is in a computer programming language,

a blending mechanism configured to blend the first portion and the second portion into an executable simulation; and

an executing mechanism configured to execute the executable simulation, wherein executing the executable simulation allows a designer to simulate operation of the digital circuit.

44. (New) The apparatus of claim 43, further comprising a mapping mechanism configured to map data types native to the hardware description language to data types native to the computer programming language.

45. (New) The apparatus of claim 43, further comprising a creating mechanism configured to create a wrapper for code written in the computer programming language so that code written in the hardware description language can call code written in the computer programming language.

46. (New) The apparatus of claim 45, further comprising a communication mechanism configured to communicate between code written in the hardware description language and code written in the computer programming language.

47. (New) The apparatus of claim 45, wherein the wrapper is automatically generated.

48. (New) The apparatus of claim 45, wherein the wrapper provides automatic threading.

49. (New) The apparatus of claim 48, wherein automatic threading enables code written in the computer programming language to call code written in the hardware description language.

50. (New) The apparatus of claim 45, wherein the wrapper can output a message upon an occurrence of a call and a return, wherein the message can include values associated with the call and the return.